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NEUTRAL-POINT-CLAMPED BOOST TRANSFORMER-LESS MULTILEVEL INVERTER FOR SOLAR PV APPLICATION

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ABSTRACT: Transformer-less multilevel inverters (MLI) are most popular in photovoltaic applications. In such system, a significant leakage current flows that needs to be reduced. One of the method being the common-ground structure and the other most popular is the active neutral-point-clamping (NPC) method, which reduces the common-mode voltage and thus the leakage current. Voltage boosting using minimum number components is also another key requirement. This work proposes a 7-level single-input transformer-less NPC MLI using switched-capacitor (SC) concept. The SC are charged to the input voltage magnitude in parallel and discharged in series, which retains the self-voltage balancing ability. The SC voltage and the dc-link voltage in combination thus produce 1.5 times boosted output. The voltage stress in the proposed topology is also limited to input voltage magnitude. Compared to the recently developed 7-level similar topologies, the proposed topology has lower conduction loss and higher efficiency. Detailed simulations are carried out under change in modulation index, load variation, change in supply input and change in load frequency, to validate the efficacy of the proposed MLI.

KEYWORDS

Boost multilevel inverter, Neutral-point-clamping, Reduced switch, Single-input, Seven-level, Switched-capacitor, Voltage-balancing

Introduction

Emergence of green energy utilization in the energy sector has put forward rigorous development of new power electronic converters in the recent years (Pawar, 2019). Green energy sources such as photovoltaic (PV), wind, etc. are more popular for impactful energy generation and utilization (Joshi et al., 2017; Shah, 2018). In such systems, dc-dc converter and dc-ac converters are the heart of the systems. The two stage system generally includes and dc-dc stage and recently developed single-stage systems avoids dc-dc stage (Budhrani et al., 2018; Sen et al., 2019). A single-stage system also avoids a high-cost transformer and such transformer-less single-stage PV systems thus need an inherent boosting ability. Inherent boosting ability can be achieved by designing boost type inverters and recent-art multilevel inverters (MLIs) are one of such types (Bana et al., 2019; Bharath et al., 2020).

Conventionally, MLIs are cascaded H-bridge (CHB) type, flying capacitor (FC) based and neutral-point-clamped (NPC) type. All the three topologies have been widely deployed in PV systems to improve the power quality and efficiency (Bana et al., 2019; K. P. Panda, Anand, et al., 2018). More number of components has been a major concern in conventional MLIs and thus in (K. P. Panda et al., 2019; K. P. Panda & Panda, 2018) new structures have been introduced with reduced number of components. Structures in (K. P. Panda, Bana, et al., 2018; K. P. Panda et al., 2020b) are other such types of MLI that reduces the number of switches. These structures are competitive with respect to high-level output generation. However, the switch count with respect to number of levels and the source count with respect to number of levels is very high. These structures are based on H-bridge and require multiple numbers of sources. More number of sources imposes issues on controlling each of the individual panels in PV application. Another concern is the absence of boosting feature in conventional MLIs, which is a mandatory requirement in PV application when feeding power to the load or utility grid. Only suitable solution to

design a transformer-less dc-ac converter with inherent boosting feature is switched-capacitor (SC) based MLIs.

SC MLIs have been a recent emerging alternative that is highly suitable for PV and high-frequency applications. Structures in (Babaei & Gowgani, 2014; Hinago & Koizumi, 2012) requires a single-source to produce a boosted output utilizing reduced number of components than the conventional structures. The SCs used in the circuit are charged in parallel and discharge in series, which enables maintaining of the required voltage in the continuous operation. The basic modules in these MLIs produce a 5-level (5L) output using two switches, one capacitor and a diode. A key advantage is the self-balancing and boosting ability of the capacitors, which does not burden the control design. Significant reduction in number of switches is still possible using (K. P. Panda et al., 2020c; Peng et al., 2019). These structures produce a 7-level (7L) output using single-source and a few capacitors. Both structures can be suitably extended to synthesize higher voltage levels at the output. Similar other SC MLIs proposed in (Khan et al., 2020; K. P. Panda et al., 2022) are extendable to higher levels. Although these MLIs need fewer switches, but requires a full-bridge along with a basic module to produce the 7L output. The four switches in the full-bridge sums up to a high voltage stress, which needs special attention. To produce high-quality output while avoiding the full-bridge, 13-level (13L) structures proposed in (K. P. Panda et al., 2020a; P. Panda et al., 2020) are the best alternatives. Using single-source the three to six-times voltage boosting is possible using minimum number of capacitors and reduced switch count compared to recent-art topologies.

The above-disclosed topologies have different advantages as mentioned. However, with respect to integrating with single-stage grid-tied PV systems another key concern is the leakage current. None of the structures discussed above as the ability to reduce the leakage current by keeping the common mode voltage minimum. Leakage current magnitude though very less can introduce significant issues in the system as well as impose restrictions to the customers. Retaining all the advantages, a straight-forward solution to get rid of the leakage current is enabling a common-grounded (CG) connection (Barzegarkhoo et al., 2021) and NPC type connection (K. P. Panda et al., 2020d). Fig. 1 shows the generalized presentation of both these types of transformer-less MLIs. As can be clearly seen, the ac neutral is connected to negative of the dc-link in CG MLIs and the ac neutral is connected to the common dc-link neutral clamping point.

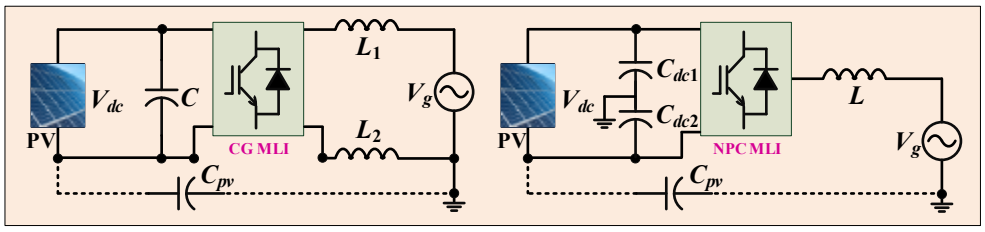


Figure 1: Generalized design of transformer-less MLI

Active NPC type SC MLIs have been proposed with an aim to utilize in transformer-less PV systems. The structure in (Siwakoti et al., 2019) is one such type, which has the disadvantage of voltage boosting while generating a 7L output. With regard to voltage boosting, which is an essential requirement, NPC type boost structures (NPC-B-MLI) in (Lee et al., 2019, 2020; Lee & Lee, 2019; Sathik et al., 2019) are the improved alternative topologies. These structures need reduced number of switches and a single input voltage. Some structure has high voltage stress and the other MLI has high rating of the capacitors. A most compact structure recently proposed in (K. P. Panda et al., 2020d) that has all the discussed advantages. With this motivation, this work proposes a 7L NPC-B-MLI with maximum advantages for utilization in single-stage PV systems.

The operational analysis of the proposed MLI is carried out in the Section 2, which also includes the design guidelines and voltage balancing investigation in detail. A comparative summary is included in Section 3 to justify the benefits of newly developed structure. Section 4 analyzes the results using MATLAB simulations. At the end, conclusions are drawn.

2. Design and Operation of the Proposed NPC-B-MLI

Fig. 2 shows the proposed 7L NPC-B-MLI topology consisting of one input source (V_{dc}), 2 dc-link capacitors (C_{dc1} & C_{dc2}), two switched capacitors (C_1 & C_2), 4 diodes (D_1 – D_4) and 7 switches (S_1 – S_7). One of the switches S3 is a bidirectional switch and all other switches are unidirectional.

An inductor L is additionally connected in the charging path of the SCs, which plays an important role in reducing the high current spikes in capacitor arises due to the potential difference between the source voltage and steady-state capacitor voltage. The switches S_1 – S_3 conducts only once in each half-cycles. On the other hand, switches S_4 & S_5 conducts completely in the positive half cycle and S_6 & S_7 conducts only in the negative half cycle. In this way, the proposed MLI produces 7 level output with 0, ±0.5V_{dc}, ±V_{dc}, ±1.5V_{dc} levels.

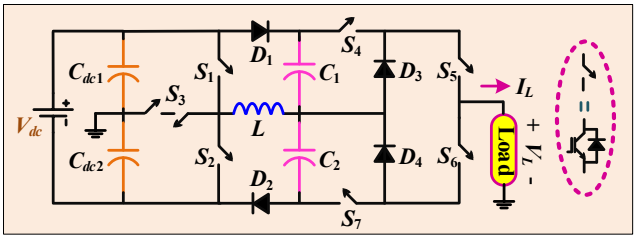


Figure. 2: Proposed 7-level NPC-B-MLI

Considering the steady-state voltage across the dc-link capacitors as $V_{dc}/2$ and the steady-stage voltage across the SCs as V_{dc}, the circuit operation is analyzed. The zero level is synthesized due to the conduction of the bidirectional switch S_3 and alongside the switches S_5 and S_6 turned on to freewheel the load current. The capacitors are idle under this condition. As stated earlier, switches S_4 & S_5 conducts completely in the positive half cycle and S_6 & S_7 conducts only in the negative half cycle. The SCs C_1 and C_2 are charged while the dc-link capacitor produces the first level of output, i.e., +0.5V_{dc} and -0.5V_{dc}, respectively due to conduction of S_2 and S1 additionally in the positive and negative half cycles. The bidirectional switch conducts in the next level during ±V_{dc} and only the SCs are accountable for generation of this voltage level. The peak voltage level is produced by turning on S_1 and S_2 additionally in the positive and negative half cycles. Both the dc-link capacitor and SC are accountable for generation of the peak voltage level ±1.5V_{dc}. The equivalent circuit in each level is shown in Fig. 3 without the inductor, as the selected value of the inductor is very small.

V_L	On switch (1) and Off switch (0)						
	S_1	S_2	S_3	S_4	S_5	S_6	S_7
1.5V_{dc}	1	0	0	1	1	0	0
1V_{dc}	0	0	1	1	1	0	0
0.5V_{dc}	0	1	0	1	1	0	0
0	0	0	1	0	1	1	0
-0.5V_{dc}	1	0	0	0	0	1	1
-1V_{dc}	0	0	1	0	0	1	1
-1.5V_{dc}	0	1	0	0	0	1	1

Table 1: Conduction of the Switches to Generate 7L Output

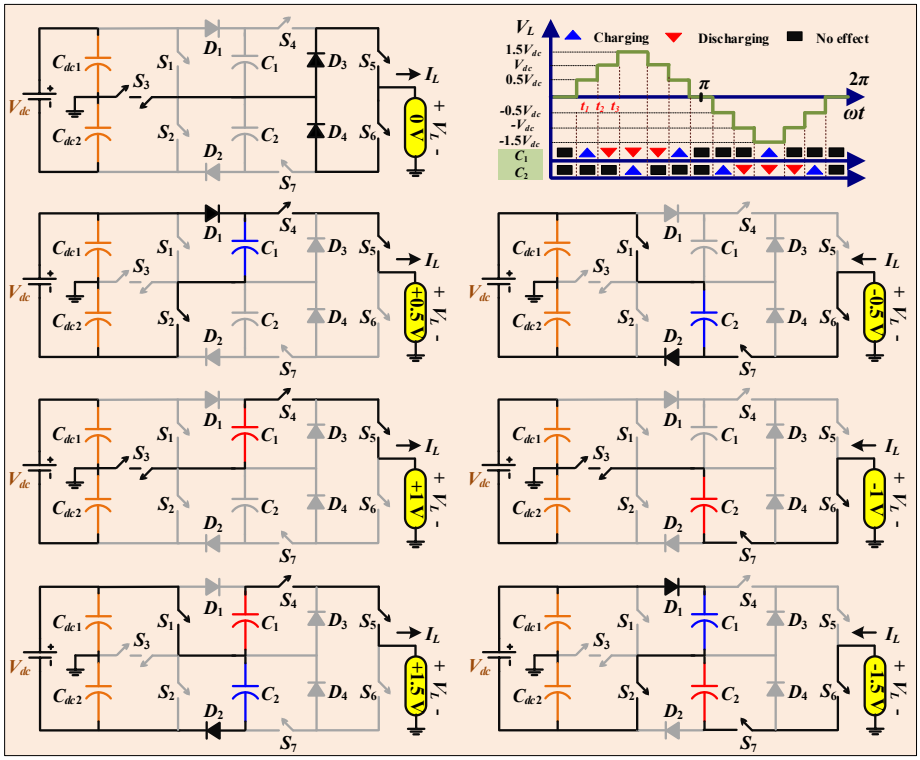


Figure 3: Operational Modes Of The Proposed 7-Level Npc-B-Mli

2.1 Self-voltage Balancing Analysis

The capacitor C_2 are charged when S_1-D_2 conducts simultaneously and similarly C_1 is charged when S_2-D_1 conducts simultaneously. Both these capacitors are charged to V_{dc} in parallel with the dc source and discharged in series with the source within a cycle of conduction. In other words, both capacitors charging-discharging duration is sufficiently less than one full cycle. This in turn enables self-balancing of the voltage across SCs. On the other hand, the input voltage is divided equally across the dc-link capacitors due to type of connection. Thus, the steady-state voltage across the dc-link capacitors is $V_{dc}/2$. This proves all the capacitors used in the proposed circuit are self-balanced type and does not require any additional control circuit for voltage balancing.

2.2 Design Guidelines

The capacitors in the proposed MLI are responsible for voltage levels generation. Therefore, the capacitor ratings and sizing is a key factor for smooth operation of the proposed MLI. Considering the duration of discharging of the capacitors, the voltage ripple (ΔV_c) and the peak load current (ILp), SCs can be selected. From Fig. 3, both the SCs discharge for the same duration that is during [t_2 to π-t_2]. Therefore, supposedly considering a voltage ripple of (x = 5%), the capacitance of the SCs (C_1 or C_2) is expressed as follows:

$$C \geq \frac{\Delta Q_C}{\Delta V_C} = \frac{2I_{Lp}\cos t_2 \cos \Phi}{x\omega V_{dc}}$$

where ΔQc is the discharging quantity, Φ is the phase angle and ω = 2πfo.

On the other hand, the dc-link capacitors carry equal voltage and current as per the connection. Considering the peak load current ILp is flowing in the dc-link capacitors, the capacitance (Cdc1 or Cdc2) can be calculated as,

$$C_{dc} = \frac{\Delta Q_{dc}}{\Delta V_{dc}} = \frac{I_{Lp}}{\omega \Delta V_{dc}}$$

where ΔQdc is the discharging quantity and ΔVdc is the voltage ripple across the dc-link capacitors.

Comparative Analysis with Existing Boost Type MLIs

To justify the advantages of the proposed MLI, similar topologies developed recently are taken into comparative analysis. All the structures require a single dc source to produce 7L output of 1.5 times the voltage gain. In terms of number of switches, the proposed MLI requires minimum number of switches similar to the structure (K. P. Panda et al., 2020d). Only 7 drivers are required, which is also minimum compared to the existing MLIs. In terms of number of switches in the conducting path, the proposed MLI is superior as it is minimum. This indicates lower conduction loss in the proposed topology. Minimum voltage stress is another key advantage of the proposed MLI. The peak voltage stress is not more than the input voltage. These advantages clearly indicate the superiority of the proposed MLI in single-stage transformer-less PV application.

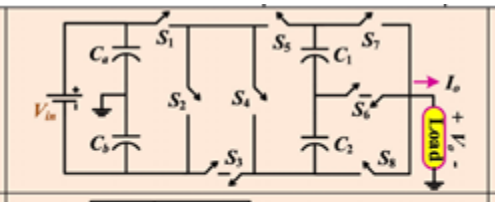
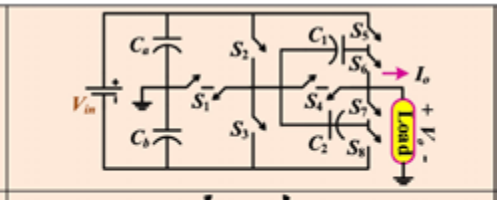
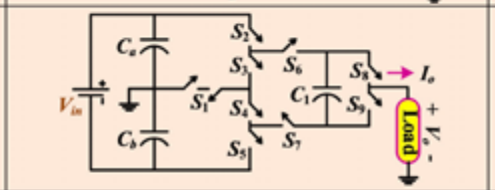
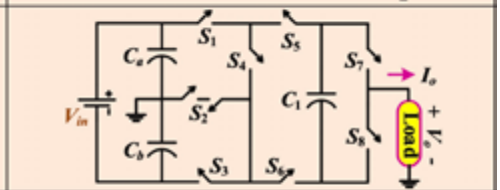
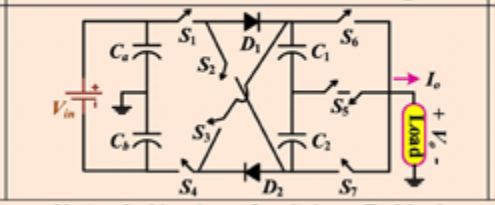
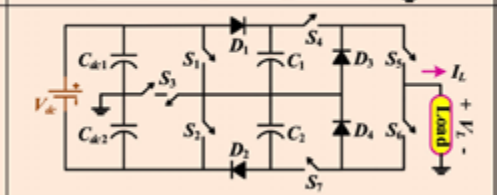
MLI in (Lee et al., 2019) A = 10 B = 6		MLI in (Lee & Lee, 2019) A = 10 B = 5	
MLI in (Sathik et al., 2019) A = 10 B = 5		MLI in (Lee et al., 2020) A = 9 B = 5	
MLI in (K. P. Panda et al., 2020d) A = 8 B = 4		Proposed MLI A = 8 B = 3	
Note: **A:** Number of switches, **B:** Maximum number of switches in the conducting path			

Table 2: Comparison of the Proposed MLI with Similar 7-level Structures

Simulation results

Simulations are carried out in Simulink platform to verify the correct functioning of the proposed MLI. Several modulation schemes have been disclosed in the literature (Bana et al., 2019; K. P. Panda et al., 2020b). Fundamental switching schemes are easier to implement, whereas carrier-based modulation techniques are useful in closed-loop control systems. The objective of the work here is to justify the operation ability only. Therefore, using a fundamental frequency modulation, switching angles are pre-computed and used for pulse generation. The topology is designed in simulink with an input voltage of 100 V and for an output frequency of 50 Hz. The dc-link capacitor values are 1500 μF and the SCs of 2200 μF are selected. A small inductor of 8 μH is used in the circuit. Fig. 4 shows the output with continuous change in modulation index from time to time. The switching angles are stored in form of a look-up table for each modulation index before they are processed. At higher modulation index of 0.95, THD is about 10 % and THD goes on increasing from 15 % to 19 % with reduction in modulation index from 0.65 to 0.1. Note that, the capacitor voltages are balanced at the steady state voltage in the ratio of 1:2.

Further, to justify the self-voltage balancing and voltage boosting ability, the input voltage change is applied as in Fig. 5 from 80 V to 100 V. The capacitor tracks the required voltage naturally. The SC voltages changes from almost 80 V to 100 V, whereas the dc-link capacitor voltages balances inherently. In this way, the peak output voltage changes from almost 120 V to 150 V smoothly. This result is taken under a steady-state resistive-inductive (RL = 50 ohm – 0.2 H) loading.

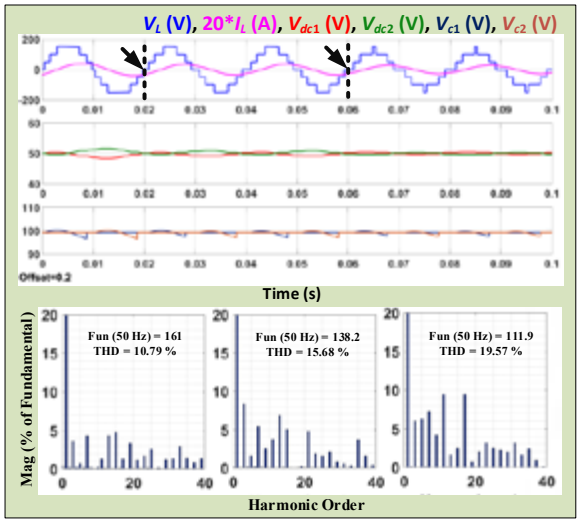


Figure 4: Results under a change in modulation index

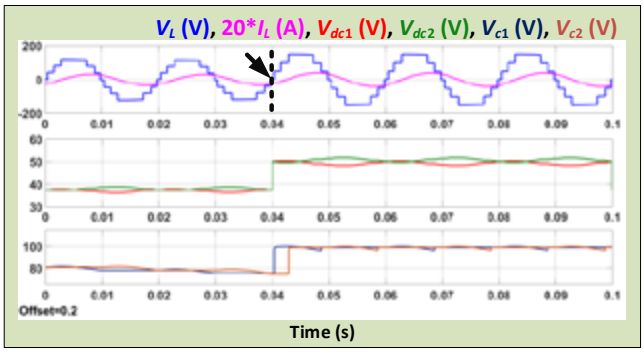


Figure 5: Results under sudden increase in input voltage

Sudden change in load is inevitable for inverter integrated systems. Considering this, first the load is varied from resistive (R = 80 ohm) to resistive-inductive (RL = 50 ohm – 0.2 H) loading. As can be seen from Fig. 6, the load current changes the pattern from staircase type to sinusoidal type. The SC voltage ripple reduces and the ripple in dc-link increase with a decrease in loading. Similar, results are observed when the load changes from 120 ohm – 0.1 H to 50 ohm – 0.2 H. It can be noticed that, the 7-level and 1.5 times boosted load voltage is unaffected.

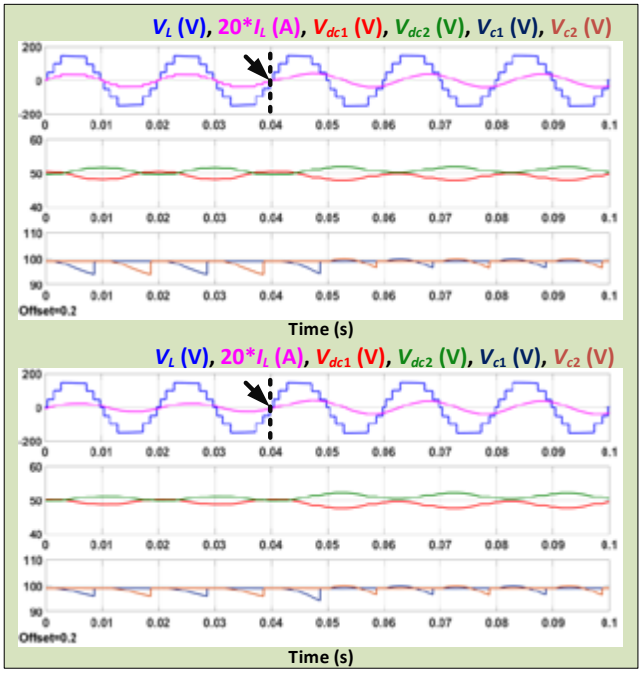


Figure 6: Results under sudden change in loading

Fig. 7 shows the results under change in load frequency. SC type MLIs will be useful in high-frequency applications as the charging current reduces at high frequency. As the frequency changes from 50 Hz to 100 Hz, load voltage changes and the capacitor voltage reduces notably. With an inductor in the charging loop, the charging current with 50 Hz load frequency is very low. Also, with 100 Hz load frequency the capacitor current drops to a very low value.

Fig. 8 shows the voltage stress across each of the switches, power losses and efficiency. Voltage stress across all the switches is limited to the magnitude of input voltage. It can also be verified that except the switch S3, all other switches are unidirectional. Further, the switching loss (PsL), conduction loss (PcL) and the ripple loss in capacitors (PrL) that majorly contributes to the total power loss is evaluated by detailed circuit simulation. The power loss increases with increase in output power, but the efficiency of the proposed circuit is preserved more than about 95 %.

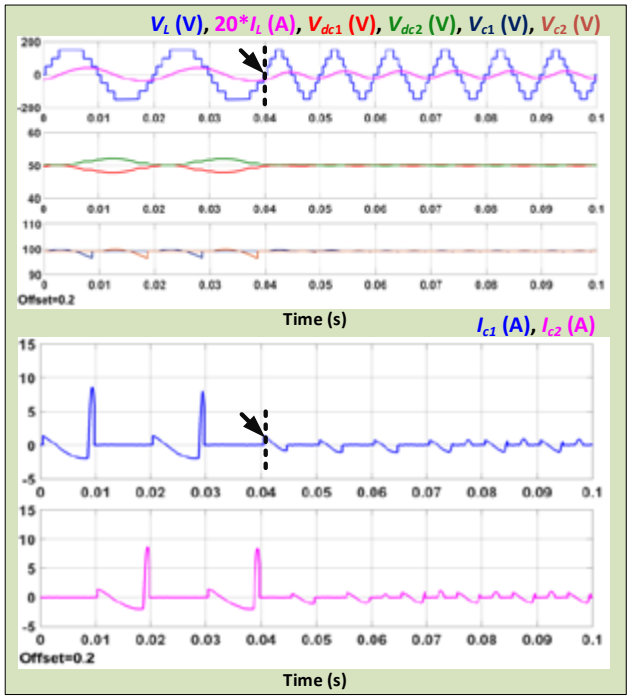


Figure 7: Results under increase in load frequency

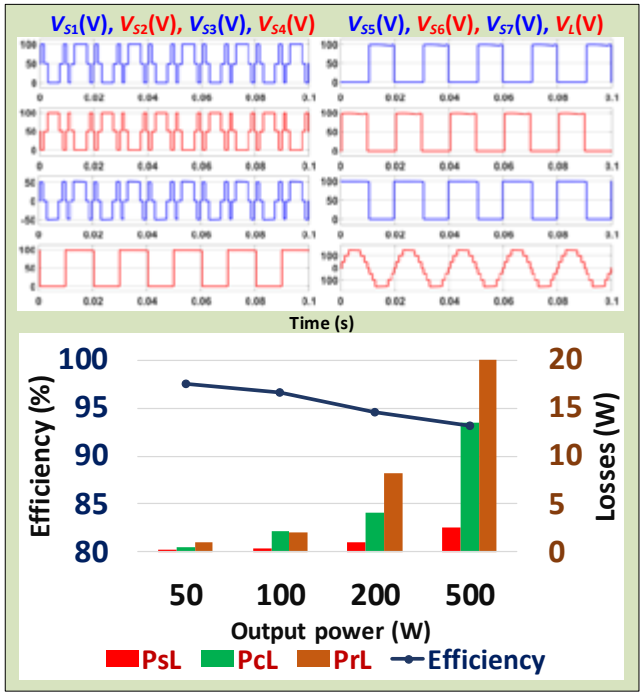


Figure 8: Voltage stress and Efficiency evaluation

Conclusion

This work has introduced a novel NPC MLI based on SC concept suitable for transformer-less PV application. NPC connection reduces the common-mode voltage and therefore, the leakage current issue is resolved. The proposed MLI consists of a single-source and reduced number of components that synthesizes a 7-level output. The SC assists in voltage boosting to 1.5 times by maintaining the desired voltage across it inherently. Therefore, control complexity is simplified. The voltage stress across the switches is kept within the limit of the input voltage magnitude that avoids the design complexities in high-voltage application. The detailed operation of the circuit in different mode shows that the proposed MLI can work effectively under any load power factor. Additionally, only a maximum of three-switches are in conduction in any level, which maintains lower power loss. All these advantages have been verified through detailed comparison with state-of-art 7-level NPC-type boost MLIs. Simulation results under different condition justify the operation under low-high modulation index, different loading condition and change in input voltage.

References

Babaei, E., & Gowgani, S. S. (2014). Hybrid Multilevel Inverter Using Switched Capacitor Units. IEEE Transactions on Industrial Electronics, 61(9), 4614–4621.

Bana, P. R., Panda, K. P., Naayagi, R. T., Siano, P., & Panda, G. (2019). Recently Developed Reduced Switch Multilevel Inverter for Renewable Energy Integration and Drives Application: Topologies, Comprehensive Analysis and Comparative Evaluation. IEEE Access, 7, 54888–54909.

Barzegarkhoo, R., Lee, S. S., Khan, S. A., Siwakoti, Y., & Lu, D. D.-C. (2021). A Novel Generalized Common-Ground Switched-Capacitor Multilevel Inverter Suitable for Transformerless Grid-Connected Applications. IEEE Transactions on Power Electronics, 36(9), 10293–10306.

Bharath, G. V., Hota, A., & Agarwal, V. (2020). A New Family of 1-φ Five-Level Transformerless Inverters for Solar PV Applications. IEEE Transactions on Industry Applications, 56(1), 561–569.

Budhrani, A. H., Bhayani, K. J., & Pathak, A. R. (2018). Design Parameters Of Shunt Active Filter For Harmonics Current Mitigation. PDEU JOURNAL OF ENERGY AND MANAGEMENT, 2(2).

Hinago, Y., & Koizumi, H. (2012). A Switched-Capacitor Inverter Using Series/Parallel Conversion With Inductive Load. IEEE Transactions on Industrial Electronics, 59(2),

878–887.

Joshi, S., Pandya, V., & Dhandhia, A. (2017). Simulation on MPPT Based Solar PV Standalone System. PDEU JOURNAL OF ENERGY AND MANAGEMENT, 2(1).

Khan, M. N. H., Forouzesh, M., Siwakoti, Y. P., Li, L., & Blaabjerg, F. (2020). Switched Capacitor Integrated (2n + 1)-Level Step-Up Single-Phase Inverter. IEEE Transactions on Power Electronics, 35(8), 8248–8260.

Lee, S. S., Bak, Y., Kim, S.-M., Joseph, A., & Lee, K.-B. (2019). New Family of Boost Switched-Capacitor Seven-Level Inverters (BSC7LI). IEEE Transactions on Power Electronics, 34(11), 10471–10479.

Lee, S. S., & Lee, K. (2019). Dual-T-Type Seven-Level Boost Active-Neutral-Point-Clamped Inverter. IEEE Transactions on Power Electronics, 34(7), 6031–6035.

Lee, S. S., Lim, C. S., & Lee, K.-B. (2020). Novel Active-Neutral-Point-Clamped Inverters With Improved Voltage-Boosting Capability. IEEE Transactions on Power Electronics, 35(6), 5978–5986.

Panda, K. P., Anand, A., Bana, P. R., & Panda, G. (2018). Novel PWM Control with Modified PSO-MPPT Algorithm for Reduced Switch MLI Based Standalone PV System. International Journal of Emerging Electric Power Systems, 19(5).

Panda, K. P., Bana, P. R., Naayagi, R. T., & Panda, G. (2022). A Dual-Source Self-Balanced Switched-Capacitor Reduced Switch Multilevel Inverter With Extending Ability. IEEE Access, 10, 61441–61450.

Panda, K. P., Bana, P. R., & Panda, G. (2018). FPA Optimized Selective Harmonic Elimination PWM Technique Application in Reduced Switch Count Multilevel Inverter. 2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), 1–6.

Panda, K. P., Bana, P. R., & Panda, G. (2020a). A Reduced Device Count Single DC Hybrid Switched-Capacitor Self-Balanced Inverter. IEEE Transactions on Circuits and Systems II: Express Briefs, 1–1.

Panda, K. P., Bana, P. R., & Panda, G. (2020b). FPA Optimized Selective Harmonic Elimination in Symmetric–Asymmetric Reduced Switch Cascaded Multilevel Inverter. IEEE Transactions on Industry Applications, 56(3), 2862–2870.

Panda, K. P., Bana, P. R., & Panda, G. (2020c). A Self-Balanced Switched-Capacitor Boost Seven-Level Inverter for Photovoltaic Systems. 2020 IEEE International Conference on Computing, Power and Communication Technologies (GUCON), 338–343.

Panda, K. P., Bana, P. R., & Panda, G. (2020d). Reduced Switch Count Seven-level Self-Balanced Switched-Capacitor Boost Multilevel Inverter. 2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), 1–6.

Panda, K. P., Lee, S. S., & Panda, G. (2019). Reduced Switch Cascaded Multilevel Inverter with New Selective Harmonic Elimination Control for Standalone Renewable Energy System. IEEE Transactions on Industry Applications, 55(6), 7561–7574.

Panda, K. P., & Panda, G. (2018). Application of swarm optimisation-based modified algorithm for selective harmonic elimination in reduced switch count multilevel inverter. IET Power Electronics, 11(8), 1472–1482.

Panda, P., Bana, P. R., & Panda, G. (2020). A Switched-Capacitor Self-Balanced High-Gain Multilevel Inverter Employing a Single DC Source. IEEE Transactions on Circuits and Systems II: Express Briefs, 1–1.

Pawar, M. (2019). A Study On Implementation Of 'Smart Grid' Technology In Indian Power Sector. PDEU JOURNAL OF ENERGY AND MANAGEMENT, 4(1).

Peng, W., Ni, Q., Qiu, X., & Ye, Y. (2019). Seven-Level Inverter With Self-Balanced Switched-Capacitor and Its Cascaded Extension. IEEE Transactions on Power Electronics, 34(12), 11889–11896.

Sathik, M. J., Sandeep, N., & Blaabjerg, F. (2019). High Gain Active Neutral Point Clamped Seven-Level Self-Voltage Balancing Inverter. IEEE Transactions on Circuits and Systems II: Express Briefs, 1–1.

Sen, P., Bana, P. R., & Panda, K. P. (2019). Firefly Assisted Genetic Algorithm for Selective Harmonic Elimination in PV interfacing Reduced Switch Multilevel Inverter. International Journal of Renewable Energy Research (IJRER), 9(1), 32–43.

Shah, N. (2018). Analysis Of The Key Factors Affecting Levelized Cost Of Electricity Of Solar Pv In India. PDEU JOURNAL OF ENERGY AND MANAGEMENT, 3(1).

Siwakoti, Y. P., Mahajan, A., Rogers, D. J., & Blaabjerg, F. (2019). A Novel Seven-Level Active Neutral-Point-Clamped Converter With Reduced Active Switching Devices and DC-Link Voltage. IEEE Transactions on Power Electronics, 34(11), 10492–10508.